
64 Pin, 16-Bit Digital Signal Controllers with High-Resolution PWM and CAN Flexible Data (CAN FD)

Operating Conditions

- 3.0V to 3.6V, -40°C to +125°C, DC to 100 MIPS

Core: 16-Bit CPU

- 256 Kbytes of Program Flash with ECC and 24K RAM
- Fast 6-Cycle Divide
- Live Update
- Code Efficient (C and Assembly) Architecture
- 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support
- Four Sets of Interrupt Context Saving Registers which Include Accumulator and STATUS for Fast Interrupt Handling
- Zero Overhead Looping
- RAM Memory Built-In Self-Test (MBIST)

Clock Management

- Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Reference Clock Output
- Fail-Safe Clock Monitor (FSCM)
- Fast Wake-up and Start-up
- Backup Internal Oscillator

Power Management

- Low-Power Management Modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset

High-Speed PWM

- 8 PWM Pairs
- Up to 250 ps PWM Resolution
- Dead Time for Rising and Falling Edges
- Dead-Time Compensation
- Clock Chopping for High-Frequency Operation
- Fault and Current Limit Inputs
- Flexible Trigger Configuration for ADC Triggering

Timers/Output Compare/Input Capture

- One General Purpose Timer
- Peripheral Trigger Generator (PTG):
 - Up to 15 trigger sources to other peripheral modules
 - CPU independent state machine-based instruction sequencer
- Nine M CCP/SCCP modules which Include Timer, Capture/Compare and PWM:
 - 1 M CCP
 - 8 SCCPs
 - 16 or 32-bit time base
 - 16 or 32-bit capture
 - 4-deep capture buffer
- Fully Asynchronous Operation, Available in Sleep Modes